The documentation and process conversion measures necessary to comply with this revision shall be completed by 8 April 2016.

INCH-POUND

MIL-PRF-19500/501F 8 January 2016 SUPERSEDING MIL-PRF-19500/501E 4 September 2013

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, DARLINGTON, PNP, SILICON, POWER, ENCAPSULATED (THROUGH-HOLE MOUNT PACKAGE), TYPES 2N6051 AND 2N6052, QUALITY LEVELS JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

- * 1.1 <u>Scope</u>. This specification covers the performance requirements for PNP, Darlington, silicon, power transistors. Three levels of product assurance (JAN, JANTX, and JANTXV) are provided for each encapsulated device.
- * 1.2 <u>Package outlines</u>. The device package outlines are as follows: TO-3 in accordance with figure 1 for all encapsulated device types.
 - 1.3 Maximum ratings. Unless otherwise specified, $T_C = +25^{\circ}C$.

Туре	P _T (1)	P _T (1)	$R_{ hetaJC}$	V_{CBO}	V_{CEO}	V_{EBO}	Ic	Ι _Β	T _J and T _{STG}
Туре	T _C = +25°C	T _C = +100°C							
	W	W	<u>°C/W</u>	V dc	V dc	V dc	A dc	A dc	<u>°C</u>
2N6051 2N6052	150 150	75 75	1.0 1.0	-80 -100	-80 -100	-5 -5	-12 -12	-0.2 -0.2	-55 to +175 -55 to +175

(1) Derate linearly at 1.00 W/°C above T_C > +25°C (see figure 2).

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil/.

AMSC N/A FSC 5961

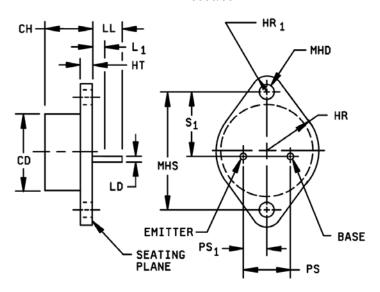


1.4 <u>Primary electrical characteristics</u>. Unless otherwise specified, $T_C = +25$ °C.

	h _{FE2} (1)	h _{FE3} (1)	h _{fe}	h _{fe}	C _{obo}	Pulse re	sponse
Limit	$V_{CE} = -3 \text{ V dc}$ $I_{C} = -6 \text{ A dc}$	$V_{CE} = -3 \text{ V dc}$ $I_{C} = -12 \text{ A dc}$	$V_{CE} = -3 \text{ V dc}$ $I_{C} = -5 \text{ A dc}$ $f = 1 \text{ kHz}$	$V_{CE} = -3 \text{ V dc}$ $I_{C} = -5 \text{ A dc}$ $f = 1 \text{ MHz}$	100 kHz \leq f \leq 1 MHz V_{CB} = -10 V dc I_E = 0	t _{on}	t _{off}
					<u>pF</u>	<u>μS</u>	<u>μS</u>
Min	1,000	150	4 000	10	000	2	40
Max	18,000		1,000	250	300	2	10

Limit	$V_{BE(sat)}$ $I_{C} = -12 \text{ A dc}$ $I_{B} = -120 \text{ mA dc}$ (1)	$V_{CE(sat)1}$ $I_{C} = -12 \text{ A dc}$ $I_{B} = -120 \text{ mA dc}$ (1)	$V_{CE(sat)2}$ $I_{C} = -6 \text{ A dc}$ $I_{B} = -24 \text{ mA dc}$ (1)
	V dc	V dc	<u>V dc</u>
Min Max	-4.0	-3.0	-2.0

- (1) Pulsed see 4.5.1.
- * 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.
- * 1.5.1 <u>JAN certification mark and quality level for encapsulated devices</u>. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", and "JANTXV".
- * 1.5.2 <u>Device type</u>. The designation system for the device types of transistors covered by this specification sheet are as follows.
- * 1.5.2.1 <u>First number and first letter symbols</u>. The transistors of this specification sheet use the first number and letter symbols "2N".
- * 1.5.2.2 <u>Second number symbols</u>. The second number symbols for the transistors covered by this specification sheet are as follows: "6051" and "6052".
- * 1.5.3 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.



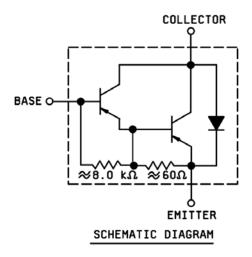


FIGURE 1. Physical dimensions (TO-3) and schematic circuit.

Ltr	Inc	hes	Millim	Notes	
	Min	Max	Min	Max	
CD		.875		22.23	3
CH	.250	.328	6.35	8.33	
HR	.495	.525	12.57	13.34	
HR ₁	.131	.188	3.33	4.78	6
HT	.060	.135	1.52	3.43	
LD	.038	.043	0.97	1.09	4, 5, 9
LL	.312	.500	7.92	12.70	4, 5, 9
L ₁		.050		1.27	5, 9
MHD	.151	.161	3.84	4.09	7
MHS	1.177	1.197	29.90	30.40	
PS	.420	.440	10.67	11.18	
PS ₁	.205	.225	5.21	5.72	5
S ₁	.655	.675	16.64	17.15	

NOTES:

- 1. Dimensions are in inches.
- 2. Millimeters are given for general information only.
- 3. Body contour is optional within zone defined by CD.
- 4. These dimensions shall be measured at points .050 inch (1.27 mm) to .055 inch (1.40 mm) below seating plane. When gauge is not used, measurement shall be made at seating plane.
- 5. Both terminals.
- 6. At both ends.
- 7. Two holes.
- 8. The collector shall be electrically connected to the case.
- 9. LD applies between L₁ and LL. Lead diameter shall not exceed twice LD within L₁.
- 10. The seating plane of the header shall be flat within .001 inch (0.03 mm), concave to .004 inch (0.10 mm), convex inside a .930 inch (23.62 mm) diameter circle on the center of the header, and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm), convex overall.
- 11. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.

FIGURE 1. Physical dimensions (TO-3) and schematic circuit - Continued.

2. APPLICABLE DOCUMENTS

- 2.1 <u>General</u>. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.
 - 2.2 Government documents.
- 2.2.1 <u>Specifications, standards, and handbooks</u>. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

- * (Copies of these documents are available online at http://quicksearch.dla.mil/).
 - 2.3 <u>Order of precedence</u>. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.
 - 3. REQUIREMENTS
 - 3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.
 - 3.2 <u>Qualification</u>. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).
 - 3.3 <u>Abbreviations, symbols, and definitions</u>. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.
 - 3.4 <u>Interface and physical dimensions</u>. The interface and physical dimensions shall be as specified in <u>MIL-PRF-19500</u> and on figure 1 herein.
 - 3.4.1 <u>Lead finish</u>. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).
 - 3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.
 - 3.6 <u>Electrical performance characteristics</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in paragraph 1.3, 1.4, and table I.
 - 3.7 <u>Electrical test requirements</u>. The electrical test requirements shall be as specified in table I.
 - 3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

- 4. VERIFICATION
- 4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:
- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and table I and II).
- 4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.
- 4.2.1 <u>Group E qualification</u>. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.
- 4.3 <u>Screening (JANTX and JANTXV levels)</u>. Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement JANTX and JANTXV levels only
(1) 3c	Thermal impedance (see 4.3.2).
9	I _{CEX1}
11	I_{CEX1} , h_{FE2} . Subgroup 2 of table I herein; $\Delta I_{CEX1} = 100$ percent of initial value or -2 μA dc, whichever is greater.
12	See 4.3.1.
13	Subgroup 2 of table I herein; $\Delta I_{CEX1} = 100$ percent of initial value or- 2 μA dc, whichever is greater; $\Delta h_{FE2} = \pm 40$ percent of initial value.

- (1) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.
- 4.3.1 Power burn-in conditions. Power burn-in conditions are as follows:

$$T_J = +162.5^{\circ}C \pm 12.5^{\circ}C; V_{CE} \ge -10 \text{ V dc}, T_A \le +100^{\circ}C.$$

NOTE: No heat sink or forced air cooling on the devices shall be permitted.

* 4.3.2 <u>Thermal impedance</u>. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). See table III, group E, subgroup 4 herein.

- 4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.
- 4.4.1 <u>Group A inspection</u>. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500, and table I herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.
- * 4.4.2 <u>Group B inspection</u>. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIB (JAN, JANTX and JANTXV) of <u>MIL-PRF-19500</u> and as follows. Delta measurements shall be in accordance with table II herein.
- * 4.4.2.1 Quality levels JAN, JANTX and JANTXV, table E-VIB of MIL-PRF-19500.

	Subgroup	<u>Method</u>	Conditions
*	В3	1037	$V_{CB} \ge -10 \text{ V dc}$; ΔT_J = between cycles $\ge +100^{\circ}\text{C}$. t_{On} = t_{Off} = 3 minutes. No heat sink or forced-air cooling on the devices shall be permitted.
	B5		Not applicable.

4.4.3 <u>Group C inspection</u>. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows. Delta measurements shall be in accordance with table II herein.

	<u>Subgroup</u>	Method	Conditions
*	C2	2036	Test condition A, weight = 10 pounds (4.5 kg), t = 15 s.
	C5	3131	See 4.3.2, $R_{\theta JC} = 1^{\circ}C/W$.
*	C6	1037	$V_{CB} \ge$ -10 V dc, ΔT_J between cycles \ge +100°C, $t_{OR} = t_{Off} = 3$ minutes. No heat sink or forced-air cooling on the devices shall be permitted.

- * 4.4.4 <u>Group E inspection</u>. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified herein. Delta measurements shall be in accordance with table II herein and applies to subgroup E1 and E2.
 - 4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.
 - 4.5.1 <u>Pulse measurements</u>. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/		MIL-STD-750	Symbol	Lir	mit	Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical examination	2071					
Subgroup 2						
Thermal impedance 2/	3131	See 4.3.2	$Z_{\theta JX}$			°C/W
Breakdown voltage collector to emitter 2N6051	3011	Bias condition D; I _C = -100 mA dc, pulsed (see 4.5.1)	V _{(BR)CEO}	-80		V dc
2N6052				-100		V dc V dc
Collector to emitter cutoff current	3041	Bias condition A; V _{BE} = +1.5 V dc	I _{CEX1}			
2N6051 2N6052		V _{CE} = -80 V dc V _{CE} = -100 V dc			01 01	mA dc mA dc
Collector to emitter cutoff current	3041	Bias condition D	I _{CEO}		-1	mA dc
2N6051 2N6052		V _{CE} = -40 V dc V _{CE} = -50 V dc				
Emitter to base cutoff current	3061	Bias condition D; V _{BE} = -5 V dc,	I _{EBO}		-2	mA dc
Base to emitter non-saturated	3066	Test condition B; I_C = -6 A dc, V_{CE} = -3 V dc, pulsed (see 4.5.1)	V _{BE}		-2.8	V dc
Base to emitter saturated	3066	Test condition A; I_C = -12 A dc, I_B = -120 mA dc, pulsed (see 4.5.1)	V _{BE(sat)}		-4.0	V dc
Collector to emitter saturated voltage	3071	I_C = -12 A dc; I_B = -120 mA dc pulsed (see 4.5.1)	V _{CE(sat)1}		-3.0	V dc
Collector to emitter saturated voltage	3071	I_C = -6 A dc; I_B = -24 mA dc, pulsed (see 4.5.1)	V _{CE(sat)2}		-2.0	V dc
Forward current transfer ratio	3076	$V_{CE} = -3 \text{ V dc}$; $I_C = -1 \text{ A dc}$, pulsed (see 4.5.1)	h _{FE1}	1,000		
Forward current transfer ratio	3076	$V_{CE} = -3 \text{ V dc}$; $I_C = -6 \text{ A dc}$, pulsed (see 4.5.1)	h _{FE2}	1,000	18,000	
Forward current transfer ratio	3076	V_{CE} = -3 V dc; I_C = -12 A dc, pulsed (see 4.5.1)	h _{FE3}	150		

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

MIL-STD-750		Symbol	Lim	its	Unit
Method	Conditions		Min	Max	
	T _A = +150°C				
3041	Bias condition A, V _{BE} = +1.5 V dc	I _{CEX2}			
	V _{CE} = -80 V dc V _{CE} = -100 V dc			-5.0 -5.0	mA dc mA dc
	T _A = -55°C				
3076	$V_{CE} = -3 \text{ V dc}, I_{C} = -6 \text{ A dc}, \text{ pulsed}$ (see 4.5.1)	h _{FE4}	300		
3206	$V_{CE} = -3 \text{ V dc}$; $I_C = -5 \text{ A dc}$; $f = 1 \text{ kHz}$	h _{fe}	1,000		
3306	$V_{CE} = -3 \text{ V dc}, I_{C} = -5 \text{ A dc},$ f = 1.0 MHz	h _{fe}	10	250	
3236	V_{CB} = -10 V dc; I_E = 0; 100 kHz \leq f \leq 1 MHz	C_obo		300	pF
	See figure 3				
	V_{CC} = -30 V dc, I_{C} = -5 A dc, I_{B1} = -20 mA dc	t _{on}		2.0	μS
	$V_{CC} = -30 \text{ V dc},$ $I_{C} = -5 \text{ A dc}, I_{B1} = I_{B2}, = -20 \text{ mA dc}$	t _{off}		10	μS
	3041 3076 3206 3306	Method Conditions $T_{A} = +150^{\circ}C$ 3041 Bias condition A, $V_{BE} = +1.5 \text{ V dc}$ $V_{CE} = -80 \text{ V dc}$ $V_{CE} = -100 \text{ V dc}$ $T_{A} = -55^{\circ}C$ 3076 $V_{CE} = -3 \text{ V dc}, I_{C} = -6 \text{ A dc}, \text{ pulsed}$ (see 4.5.1) 3206 $V_{CE} = -3 \text{ V dc}; I_{C} = -5 \text{ A dc};$ $f = 1 \text{ kHz}$ 3306 $V_{CE} = -3 \text{ V dc}, I_{C} = -5 \text{ A dc},$ $f = 1.0 \text{ MHz}$ 3236 $V_{CB} = -10 \text{ V dc}; I_{E} = 0; 100 \text{ kHz} ≤ f ≤ 1 \text{ MHz}$ See figure 3 $V_{CC} = -30 \text{ V dc},$ $I_{C} = -5 \text{ A dc}, I_{B1} = -20 \text{ mA dc}$ $V_{CC} = -30 \text{ V dc},$ $I_{C} = -30 \text{ V dc},$	Method Conditions $T_A = +150^{\circ}C$ 3041 Bias condition A, $V_{BE} = +1.5 \text{ V dc}$ $V_{CE} = -80 \text{ V dc}$ $V_{CE} = -100 \text{ V dc}$ $V_{CE} = -100 \text{ V dc}$ $V_{CE} = -100 \text{ V dc}$ $V_{CE} = -3 \text{ V dc}$ $V_{CE} = -6 \text{ A dc}$ $V_{CE} = -3 \text{ V dc}$ $V_{CE} = -6 \text{ A dc}$ $V_{CE} = -3 \text{ V dc}$ $V_{CE} = -6 \text{ A dc}$ $V_{CE} = -3 \text{ V dc}$ $V_{CE} = -6 \text{ A dc}$ $V_{CE} = -3 \text{ V dc}$ $V_{CE} = -6 \text{ A dc}$ $V_{CE} = -3 \text{ V dc}$ $V_{CE} = -6 \text{ A dc}$ $V_{CE} = -3 \text{ V dc}$ $V_{CE} = -6 \text{ A dc}$ $V_{CE} = -3 \text{ V dc}$ $V_{CE} = -6 \text{ A dc}$ $V_{CE} = -3 \text{ V dc}$ $V_{CE} = -6 \text{ A dc}$ $V_{CE} = -3 \text{ V dc}$ $V_{CE} = -6 \text{ A dc}$ $V_{CE} = -3 \text{ V dc}$ $V_{CE} = -6 \text{ A dc}$ $V_{CE} = -3 \text{ V dc}$ $V_{CE} = -6 \text{ A dc}$ $V_{CE} = -3 \text{ V dc}$ $V_{CE} = -6 \text{ A dc}$ $V_{CE} = -3 \text{ V dc}$ $V_{CE} = -6 \text{ A dc}$ $V_{CE} = -3 \text{ V dc}$ $V_{CE} = -6 \text{ A dc}$ $V_{CE} = -3 \text{ V dc}$ $V_{CE} = -6 \text{ A dc}$ $V_{CE} = -3 \text{ V dc}$ $V_{CE} = -6 \text{ A dc}$	Method Conditions Min $T_A = +150^{\circ}C$ Icex2 3041 Bias condition A, $V_{BE} = +1.5 \text{ V dc}$ Icex2 $V_{CE} = -80 \text{ V dc}$ Icex2 $V_{CE} = -100 \text{ V dc}$ Icex2 $T_A = -55^{\circ}C$ Icex2 3076 Icex2 $V_{CE} = -3 \text{ V dc}$, $I_C = -6 \text{ A dc}$, pulsed (see 4.5.1) Icex3 $V_{CE} = -3 \text{ V dc}$, $I_C = -5 \text{ A dc}$, feet and fee	Method Conditions Min Max T _A = +150°C 3041 Bias condition A, V _{BE} = +1.5 V dc I _{CEX2} V _{CE} = -80 V dc -5.0 V _{CE} = -100 V dc -5.0 T _A = -55°C h _{FE4} 3076 V _{CE} = -3 V dc, I _C = -6 A dc, pulsed (see 4.5.1) h _{FE4} 3206 V _{CE} = -3 V dc; I _C = -5 A dc; f = 1 kHz h _{fe} 1,000 3306 V _{CE} = -3 V dc, I _C = -5 A dc, f = 1.0 MHz h _{fe} 10 250 3236 V _{CE} = -10 V dc; I _E = 0; 100 kHz ≤ f ≤ 1 C _{obo} 300 MHz See figure 3 V _{CC} = -30 V dc, I _{B1} = -20 mA dc t _{on} 2.0 V _{CC} = -30 V dc, I _E = -30 V dc, I _E = -20 mA dc V _{of} 10

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/		MIL-STD-750	Symbol	Lim	nits	Unit
	Method	Conditions		Min	Max	
Subgroup 5						
Safe operating area (dc)	3051	T_C = +25°C +10°C, -0°C, t ≥ 1s, 1 cycle, see figure 4				
Test 1		$V_{CE} = -12.5 \text{ V dc}, I_{C} = -12 \text{ A dc}$				
Test 2		$V_{CE} = -30 \text{ V dc}, I_{C} = -5 \text{ A dc}$				
Test 3 2N6051 2N6052		$V_{CE} = -70 \text{ V dc}, I_{C} = -200 \text{ mA dc}$ $V_{CE} = -90 \text{ V dc}, I_{C} = -155 \text{ mA dc}$				
Safe operating area (switching)	3053	Load condition B, (clamped inductive load), $T_A = +25^{\circ}C$, $t_r + t_f \le 1.0 \mu s$ duty cycle ≤ 2 percent, $t_p = 1 ms$, (vary to obtain I_C), $R_s = 0.1 ohms$, $R_{BB1} = 80 ohms$, $V_{BB1} = 16 V dc$, $R_{BB2} = 100 ohms$, $V_{BB2} = 1.5 V dc$, $V_{CC} = 20 V dc$, $I_C = 12 A dc$, $R_L \le 2 ohms$, $I_C = 10 mH$ (Stancor C-2688 or equivalent);				
2N6051 2N6052		clamp voltage = -80 +0, -5 V dc, clamp voltage = -100 +0, -5 V dc. Device fails if clamp voltage not reached, see figure 5				
Electrical measurements		See table I, subgroup 2				
Subgroups 6 & 7						
Not applicable						

TABLE II. Groups B, C, and E delta measurements. 1/2/3/

Step	Inspection	MIL-STD-750		Symbol	Limi	t	Unit
		Method	Conditions		Min	Max	
1	Forward - current transfer ratio	3076	V _{CE} = -3 V dc, I _C = -6 A dc, pulsed (see 4.5.1)	Δh_{FE2}	±40 percent		

^{1/} The delta measurements for table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500 are subgroups 3 and 6, see table II herein, step 1.

^{1/} For sampling plan, see MIL-PRF-19500.2/ This test required for the following end-point measurements only:

Group B, subgroups 2 and 3 (JAN, JANTX, and JANTXV).

Group C, subgroups 2 and 6. Group E, subgroup 1.

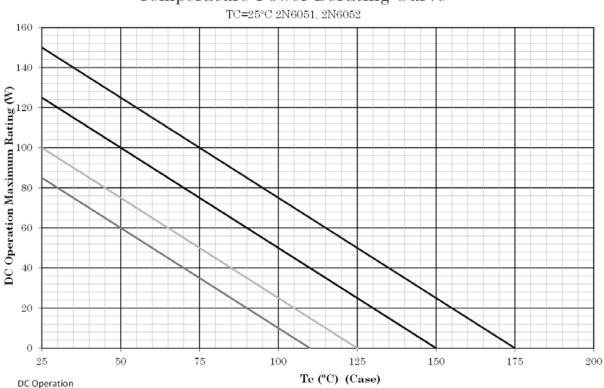
The delta measurements for table E-VII of MIL-PRF-19500 are subgroup 6, see table II herein, step 1.

The delta measurements for table E-IX of MIL-PRF-19500 are subgroup 1 and 2, see table II herein, step 1.

TABLE III. Group E inspection (all quality levels) - for qualification and re-qualification only.

Inspection		MIL-STD-750	Sample plan
	Method	Conditions	ріан
Subgroup 1			45 devices c = 0
Temperature cycling	1051	500 cycles.	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 and table II herein.	
Subgroup 2			45 devices c = 0
Blocking life	1048	Test temperature = $+125$ °C; $V_{CB} = 80$ percent rated; $T = 1,000$ hours.	
Electrical measurements		See table I, subgroup 2 and table II herein.	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	IN/A
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B.	0-0

Temperature-Power Derating Curve

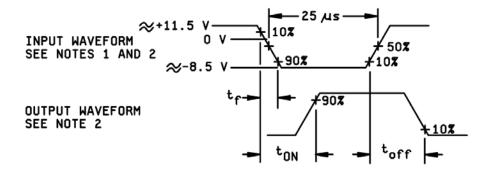


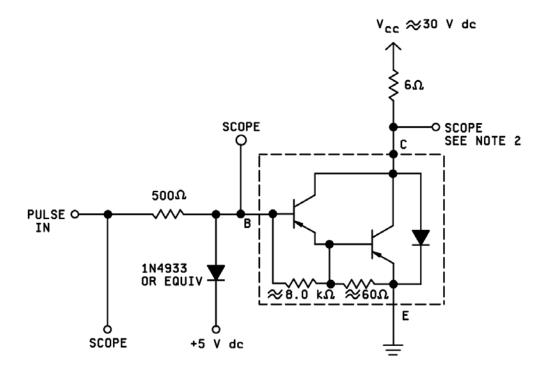
NOTES:

Thermal Resistance Junction to Case = 1.0°C/W

- This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
- 2. Derate design curve constrained by the maximum junction temperature ($T_J \le 175^{\circ}C$) and power rating specified. (See 1.3 herein.)
- 3. Derate design curve chosen at $T_J \le 150^{\circ}C$, where the maximum temperature of electrical test is performed.
- 4. Derate design curve chosen at $T_J \le 125^{\circ}C$, and $110^{\circ}C$ to show power rating where most users want to limit T_J in their application.

FIGURE 2. Temperature-power derating for 2N6051 AND 2N6052.





NOTES:

- 1. The input waveform is supplied by a pulse generator with the following characteristics: $t_{\Gamma} \le 20$ ns, $t_{f} \le 20$ ns,
- 2. Output wave forms are monitored on an oscilloscope with the following characteristics: $t_r \le 2.0$ ns, $Z_{in} \ge 20$ k Ω , $C_{in} \le 11.5$ pF.
- 3. Resistors shall be noninductive types.
- 4. The dc power supplies may require additional by-passing in order to minimize ringing.

FIGURE 3. Pulse response test circuit.

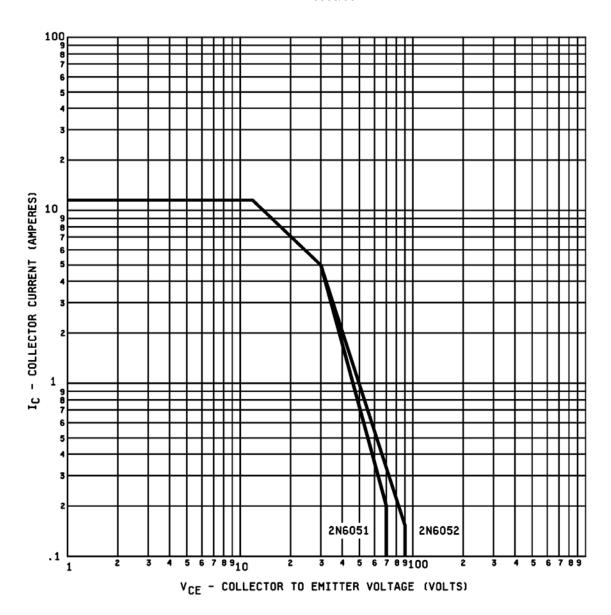


FIGURE 4. Maximum safe operating area graph (continuous dc).

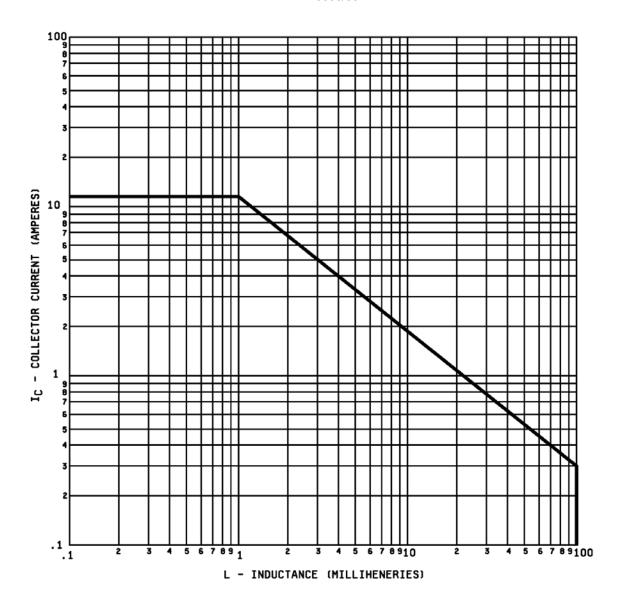


FIGURE 5. Safe operating area for switching between saturation and cutoff (unclamped inductive load).

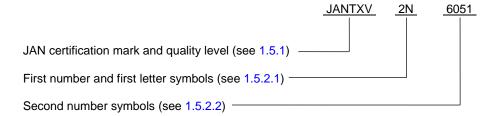
5. PACKAGING

5.1 <u>Packaging</u>. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

- 6.1 <u>Intended use</u>. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.
- * 6.2 <u>Acquisition requirements</u>. Acquisition documents should specify the following:
 - a. Title, number, and date of this specification.
 - b. Packaging requirements (see 5.1).
 - c. Lead finish (see 3.4.1).
- d. The complete PIN, see 1.5 and 6.5.
- 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.
- 6.4 <u>PIN construction example</u>.
- * 6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



- * 6.5 <u>List of PINs</u>. The following is a list of possible PINs available on this specification sheet.
- * 6.5.1 <u>List of PINs for encapsulated devices</u>. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level
JAN2N6051	JANTX2N6051	JANTXV2N6051
JAN2N6052	JANTX2N6052	JANTXV2N6052

- * 6.6 <u>Request for new types and configurations</u>. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at <u>Semiconductor@.dla.mil</u> or by facsimile (614) 693-1642 or DSN 850-6939.
 - 6.7 <u>Changes from previous issue</u>. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians: Army - CR Navy - EC Air Force - 85 NASA - NA DLA - CC Preparing activity: DLA - CC

(Project 5961-2016-007)

Review activities: Air Force - 19, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil/.